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The Functional Emulator Designs for a Memristor Model with the Programmable Analog and Digital Platforms

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Abstract

The hardware validation and verification studies about the emulator circuits of the memristor element include usually either analog or digital realization results. In this study, the implementation stages of a memristor element using Joglekar window function with programmable and reconfigurable analog and digital platformsare given togetherin order to observe the characteristic current-voltage relationship,experimentally. In here, a Joglekar window function based voltage-controlled memristor has been implemented with the Field Programmable Analog Array (FPAA) platform for the first time. In fact, the FPAA platform attracts attentions thanks to its analog nature, rapid prototyping and low hardware cost specialties and different nonlinear functionscan be constructed on this device easily. Similarly, the Field Programmable Gate Array (FPGA) platform stands out with its parallel processing feature in digital signal processing studies, recently. The FPGA-based digital implementation stages of the Joglekar window function based memristor element have been also addressed in this study. Thus, the FPAA and FPGA based memristor emulator designs are presented together in order to contribute the memristor-based analog and digital applications that is required to get real-time signals.

Keywords: Memristor, window function, reconfigurable circuit implementation, Pinch hysteresis loop, Field Programmable Analog Array (FPAA), Field Programmable Gate Array (FPGA).

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1. Introduction

In 1971, Leon Chua defined the most basic relation of the memristor elementas relating the integrals of the time-dependent electrical voltage and current signals in thebasic circuit theory[1]. This component, which is modeled as a two-terminal element and introduced as the fourth basic passive circuit element, soon attracted the attention of circuit theorists with its unique nonlinear properties that distinguish it from other passive circuit elements. Although mathematical fundamental relation of the memristor was discovered in the 1970s, the first physical realization of this element was realized forty years later by the teams of Stanley Williams and Hewlett Packard (HP) Laboratories in 2008. The remarkable features of the memristor element such as small size [2], low power consumption [3], high-speed operation [4], stable behavior [5], and multi-state operation [6]are mentioned in the report that is published by HP Company. Thus, the interest in the use of memristor elements in both scientific research and the electronics industry has increased again.

The resistance levels of this element have been used during the use of the memristor element in digital and analog electronic applications. While few resistance levels of the memristor are employed in digital electronics applications, the resistance value ranges between the minimum and maximum values are utilized for allowing actual calculation in analog applications. Several models such as Linear Ion Drift Model[7], Nonlinear Ion Drift Model[8], Simmons Tunneling Barrier Model [9], and Threshold Adaptive Memristor Model (TEAM) [10], which highlight different characteristics of the memristor element, have been defined for the electronic implementations in the literature. The Nonlinear Ion Model, which is a voltage-controlled memristor model, stands out among these models because of its more pronounced current-voltage relationship characteristic. On the other hand, it is encountered with the limit value constraints in Nonlinear Ion Modeling. This restriction is reduced by defining different window functions such as Biolek, Podromakis, Strukov, and Joglekar [11-15].

The Biolek window function model is generally approved its success because it eliminates the boundary lock problem on boundary points [16]. Although this function has offered a solution to the boundary lock problem, it cannot show continuity at the boundaries and causes the drift velocity discontinuity at the boundaries. Similar to the Biolek window function,

the Podromakis window function model has also the boundary lock problem. There are two control parameters in the Podromakiswindow function model, namely*(p)* and *(j)*.While deciding the shape of the window function with the *(p)* parameter, the scale of the amplitude of the window function can be adjusted with the *(j)* parameter.The Strukov window function model is proposed to express the behavior in the boundary conditions of the HP model. The main purpose of its proposal is to ensure that the boundary conditions of the memristor element are limited to certain special conditions. However, in the Strukov window function model, no external field effect can change the state of the memristor, which is an important problem. Additionally, it is assumed that the memristor element remembers the amount of charge. However, while the memristor remembers the boundary conditions, it will not remember the charge amount.The Joglekar window function model is proposed to overcome this shortcoming of the Strukov window function. In addition, the nonlinearity property, which is one of the basic characteristics of the memristor, is met with the Joglekar window function. Moreover, the Joglekar model is also successful in providing zero crossing and the curvature adjustment and its control can be performed with this model by using the *(p)* parameter.

After the modeling studies about the memristor element, its physical production and real-time electrical characteristic outputs have required in order to use this element in different circuits and systems. In addition to the prototype produced by HP company, several emulator circuits using different hardware have been implemented, so that the memristor element can be used in the experimental implementations. Chua [1] has utilized operational amplifiers, transistors, diodes, capacitors, resistors, and potentiometers in his first analog emulator circuit. Mutlu and Karakulak [17] have proposed another emulator circuit that includes rectifier, differential amplifier, integrator, and nonlinear resistor structures. Pershin and Di Ventra [18] have developed a programmable memristor emulator that includes a microprocessor, Analog-to-Digital Converter (ADC) and digital potentiometer. Valsa et al.[19] implemented a voltage-controlled memristor emulator that generates voltage proportional to conductivity and flux. Kim et al. [20] proposed two different memristor emulator circuits that tend to increase and decrease depending on the polarity of the applied voltage. A memristor emulator was designed by Wang et al. [21] using a light dependent resistor (LDR), their designs have been proposed for educational purposes. Biolek et al. [22] have been proposed several memristor emulators using Current Feedback Operational Amplifier (CFOA), Transimpedance Operational Amplifier

(TOA) [23]. Several different integrated components such as opamp, multiplier and complementary metal–oxide–semiconductor (CMOS) have been used for emulating memristor in the literature [24-26]. Sodhi and Gandhi [27] have designed a kit consisting of discrete elements that mimics memristor behavior and this kit can be used for educational purposes. Xudong et al.[28] have proposed a new nonlinear logarithmic model to characterize the memristor device and a memristor emulator circuit. The use of discrete hardware in many of these implementations is disadvantageous because the values of the circuit elements should be fine-tuned in these designs. For this reason, in some studies, only the analysis results of the emulator circuits, which are developed for memristors, are presented in the circuit simulation program. For example, Biolek et al. [29] have simulated the Joglekar window function by using the SPICE tool. Similarly, Adzmi et al.[30] have simulated the memristor models in SPICE tool to compare the basic characteristics of various windowing functions.

In recent years, programmable and reconfigurable analog or digital elements have attracted a lot of attention, with the features of enabling precise parameter adjustment, similar to the simplicity offered by simulation tools, and providing experimental outputs similar to measuring real-time electrical signals obtained by discrete hardware. In the literature, there have been various studies on the use of programmable and reconfigurable elements as an alternative solution for the realization of systems with different nonlinear functions. Some of these studies, in which analog or digital programmable hardware platforms have been preferred instead of using different emulator circuits for testing and verifying designs using memristor elements. For example, Tahir and Saif [31] simulated the flux-controlled memristor model numerically, they have performed the hardware implementation of this model by using a Field Programmable Analog Array (FPAA). Arık and Kılıç [32] have used a FPAA device for experimental testing and validation of the memristor-based chaotic systems.Vourkas et al.[33] have developed the first digital memristor emulator, that is based on the voltage-controlled threshold memristor model. Tomez et al. [34] have presented the Field Programmable Gate Arrays (FPGA) based implementation results of the system designing by a hybrid System Generator for three window functions based on the nonlinear dopant memristor model. Tolba et al. [35] have proposed an FPGA-based implementation for discrete memristor model (DMM) and continuous memristor model (CMM). Farooq et al. [36] have designed the basic and complex memristor-transistor hybrid building blocks of heterogeneous island-style FPGA, which are combined to form a full

hybrid heterogeneous FPGA architecture. Alombah et al.[37] have exploited the model by using three ordinary differential equations proposed by Muthuswamy [38] in 2010. The numerical analyzes of this model have been executed by using MATLAB program and it was verified by using FPGA platform.

In the literature, the hardware validation and verification studies about the emulator circuits of the memristor element include usually either analog or digital realization result [39-40]. In this study, the implementation stages of a Joglekar window function based memristor element with the programmable and reconfigurable analog and digital platforms are given together in order to observe the characteristic current-voltage relationship of the Nonlinear Ion Model, experimentally. In here, a voltage-controlled memristor modeled with the Joglekar window function has been implemented with the FPAA platform for the first time the best of our knowledge. In fact, the FPAA platform attracts attentions thanks to its analog nature, rapid prototyping and low hardware cost specialties, and having different nonlinear functions that can be constructed on this device easily. Similarly, the FPGA platform stands out with its parallel processing feature in digital signal processing recent work about studies and the FPGA-based digital implementation stages of the Joglekar window function based memristor element have been also addressed in this study. Thus, in this study, the FPAA and FPGA based memristor emulator designs are presented together in order to contribute the memristor-based analog and digital applications that require real-time signals.

In this context, in Section 2, after a short introduction to the definitions of memristance and memductance concepts, the window functions, which are defined with different functions, are examined. In order to observe the hysteresis structure, which is the characteristic curve of the memristor element, an input signal is applied to the memristor element. The memristor element exhibits frequency-dependent operating characteristics, so that these characteristics can be observed thanks to this time dependent input signal. The responses of the Joglekar window function based memristor element to the sinusoidal input signals at different frequencies are observed with the numerical simulation results. In Section 3, the details of the followed design steps for the construction of the Joglekar window function based memristor element on the FPAA platform are presented and the obtained FPAA-based implementation results are also given. During the FPAA based design process, the amplitude and the frequency of the internal

sinusoidal oscillator in the FPAA platform are set to the desired values, but there is usually no predefined sinusoidal oscillator structure in the FPGA platform. Thus, it is required to define a sinusoidal oscillator on the FPGA platform to observe characteristic outcomes of the memristor element. In this study, instead of applying an external signal from the signal generator to the FPGA platform utilizing with an analog to digital converter, a sinusoidal oscillator is built on the FPGA platform by using the Van der Pol (VDP) oscillator definition. The oscillation frequency of the VDP oscillator is adjusted to the desired frequency and it is applied to the input of the Joglekar window function based memristor element. In Section 4, the characteristic hysteresis curve of FPGA based implemented memristor element is observed, successfully. Finally, since the FPAA and the FPGA platforms are analog and digital embedded system, respectively, their typical properties cannot be directly compared. On the other hand, in addition to the followed procedures in their design stages, the bottlenecks encountered in these design stages and the proposed solution approaches to eliminate these problems, and the general outputs of these programmable platforms such as power consumption and memory usage are discussed in Section 5. The general results of this study are handled in the last section.

2. The Numerical simulation of a Joglekar window function based memristor element

Resistor, capacitor and inductor are basic passive circuit elements in circuit theory. These elements are defined by the relationship among the four circuit variables of current (i), voltage (v), electric charge (q), and magnetic flux (φ). Resistance (R)represents the relationship between

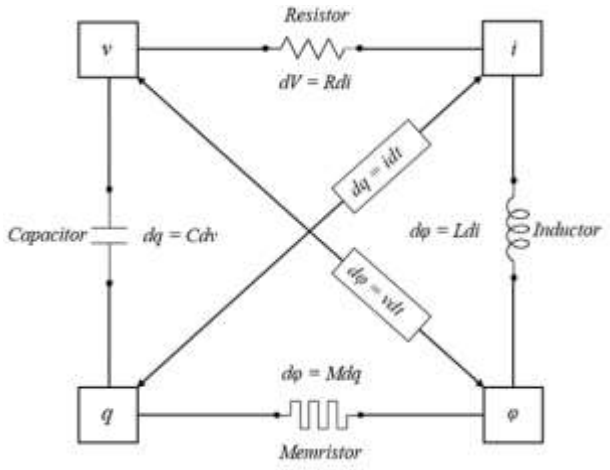


Figure 1. Relationship between basic circuit variables and basic circuit elements [7].

voltage and current ($dv=Rdi$). Capacitor (C) represents the relationship between voltage and load ($dq=Cdv$), and inductor (L) represents the relationship between current and magnetic flux ($d\varphi=Ldi$). According to Faraday's Law, current (i) is equal to the derivative of electrical charge (q) and voltage (v) is equal to the derivative of magnetic flux (φ). It is clear that there are six different combinations of the four basic circuit variables, but only five combinations are expressed according to these definitions. In the studies carried out in the 1970s, this deficiency was noticed and the fourth basic circuit element memristor was introduced [1]. The relationship between the basic circuit elements and electrical variables is shown in Figure 1.

The memristor represents the relationship between electrical charge and magnetic flux, completing the final combination. The memristor is a passive circuit element, whose resistance changes depending on the current flowing through itself. The resistance of the memristor element increases when current flows in one direction and decreases when it flows in the opposite direction. When the applied current is removed, it maintains the last resistance value until the current is applied again. This indicates that the memristor element acts as a memory resistor. The memristor, which is the abbreviation of MEMoryResISTOR, is also named because of this feature. If the relationship between charge and flux is defined as a function of charge (q), it is expressed as a charge-controlled memristor, namely called memristance, its unit is ohm (Ω) and memristanceis expressed as in Eq.(1):

$$v = M(q)i$$
$$M(q) = \frac{d\varphi(q)}{dq} \tag{1}$$

If the relationship between charge and flux is defined as a function of flux (φ), it is expressed as a flux-controlled memristor, called memductance, its unit is Siemens (S), and memductance is expressed as in Eq.(2):

$$i = W(\varphi)v$$
$$W(\varphi) = \frac{dq(\varphi)}{d\varphi} \tag{2}$$

Although memristance and memductance have units of resistance and conductivity, respectively, these elements have many unique non-linear properties such as passivity criterion, closure theorem, existence and uniqueness theorem,compressed hysteresis loops and defined limiting linear properties [41].

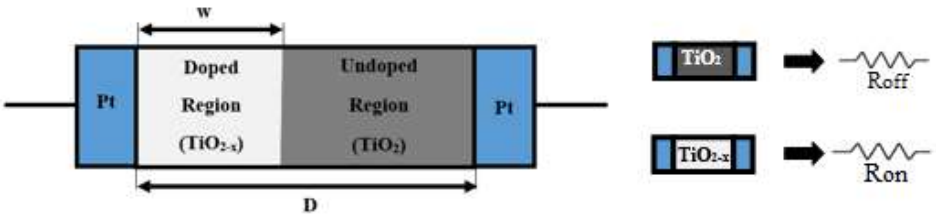


Figure 2. Memristor diagram produced by the HP company[7].

The HP company team produced the first physical memristor, namely the linear drift model. The HP memristor model is seen in Figure 2. This element have been produced by placing a thin film of titanium dioxide (TiO_2) between two platinum (Pt) electrodes [7]. In this model shown in Figure 2, (D) represents the width of the element and consists of two regions. The first region denotes the oxygen vacancies doped with positive oxygen ions, and the second region denotes the undoped portion.

The width of the doped portion is defined by (w) and has a low resistance (R_{on}). Therefore, it is more conductive. The undoped region has higher resistance (R_{off}). When $w=0$, the memristor resistance increases and acts as an open switch. When $w=D$, the memristor resistance decreases and acts as a closed switch. Considering the production process, the memristance expression of the memristor depending on the variable (w) is defined as in Eq(3):

$$M(w) = R_{on}\frac{w(t)}{D} + R_{off}(1-\frac{w(t)}{D}) \tag{3}$$

If a current $i(t)$ is applied to the memristor, the boundary between the two regions move across the memristor due to the shift of the charged dopant. Considering that there are a linear ion drift in a uniform field charge and the voltage on the memristor is defined as in Eq.(4).

$$v(t) = M(w)i(t) = \left[R_{on}\frac{w(t)}{D} + R_{off}(1-\frac{w(t)}{D})\right]i(t) \tag{4}$$

(x) is the normalized version of the variable (w) and it is defined by $x=w/D$, $x\epsilon[0,1]$. The $x(t)=0$ state corresponds to $M(x)=R_{off}$ condition and the $x(t)=1$ state corresponds to $M(x)=R_{on}$ condition. In this case, Eq. (4) can be rewritten as:

$$M(x) = R_{on}x + R_{off}(1-x)$$
$$v(t) = \left[R_{on}x + R_{off}(1-x) \right] i(t) \tag{5}$$

The electrical behavior of the memristor is related to the shift between the doped and the undoped regions and these regions are limited to the interval *[0, D]*. The situation at the boundaries is an important problem of the linear drift approach. The voltage applying to the memristor element at the nanoscale causes a large electric field that creates significant nonlinearity in ionic convection and is resulted with a rapid and significant reduction in the energy barrier [8]. This nonlinearity is manifested in the borders. That is, the ion drift velocity approaches zero and no external excitation can change the state when the memristor is set to ON or OFF. To overcome this problem, the window function approach has been introducedand this nonlinearity in the state equations has been updated in Eq. (6):

$$\frac{dx(t)}{dt} = \mu_V \frac{R_{on}}{D^2} i(t) f(x) \tag{6}$$

Depending on the structural dynamics of the memristor, we have changed the physical parameter to a fixed value, namely ($\mu_v R_{on}/D^2 \approx k$). In this case, Eq.(6) becomes in Eq.7:

$$\frac{dx(t)}{dt} = ki(t) f(x) \tag{7}$$

Several different window functions, generally defined by *f(x)* notation in Eq.(6), have been presented to the literature. Some of these functions are listed as Strukov, Joglekar, Biolek and Prodromakis window function models. The Joglekar window function has been preferred in this study because it is an improved model of the Strukov windowing function and it is simpler than the Prodromakis window function, mathematically. In 2009, Joglekar and Wolf discussed the approximate linear drift behavior and nonlinearity at the boundaries when $0 < w < D$. They checked the nonlinearity (or linearity) of their functions with a second parameter (p), that is called as the control parameter [12]. The equation proposed by Joglekar and Wolf is expressed as follow:

$$f(x) = 1 - (2x-1)^{2p} \tag{8}$$

The graph of the change of the *f(x)* function for different values of the (*p*) degree is given in Figure 3. The Joglekar model considers simple boundary conditions such as *f(0)= f(1)=0*. In the case of $p \to \infty$, the Joglekar model turns into a rectangular window function and the state variable function approaches the linear drift model (*f(0<x<1)≈1*). Therefore, in this model, *(p)* must be integers and it is generally chosen at one, two or three values.

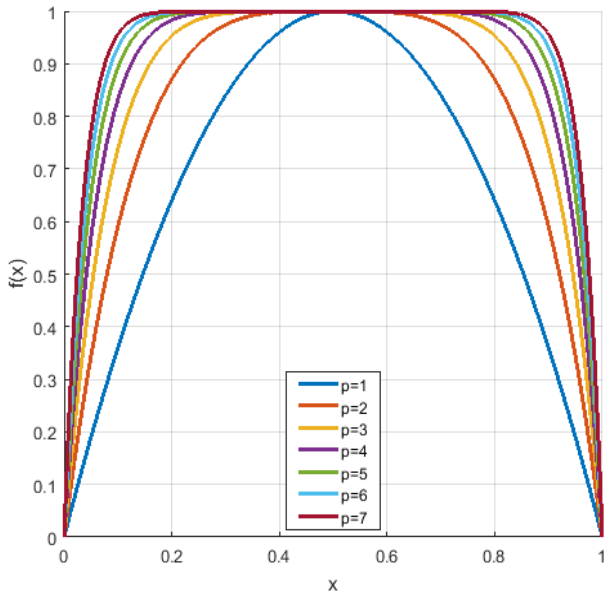


Figure 3. Graphs of the Joglekar window function for different values.

In this study, the parameters of Joglekar system are adjusted as R_{on}=*0.1 kΩ*, R_{off} =*16 kΩ*, μ_v=30.10^{-15} *m²/(V.s)*, *D*=9.10^{-9} *m* for the numerical simulation. The control parameter (*p*) is set to one. The input voltage has been selected as a sine wave with a 1V peak voltage and the frequencies at ω_1=*0.25 rad/s*, ω_2=*2.5 rad/s* and ω_3=*50 rad/s*, respectively. After applying the sinusoidal signals at different frequencies values to the input of this memristor created by using the Joglekar window function, the obtained numerical simulation results for this configuration are given in Figure 4.

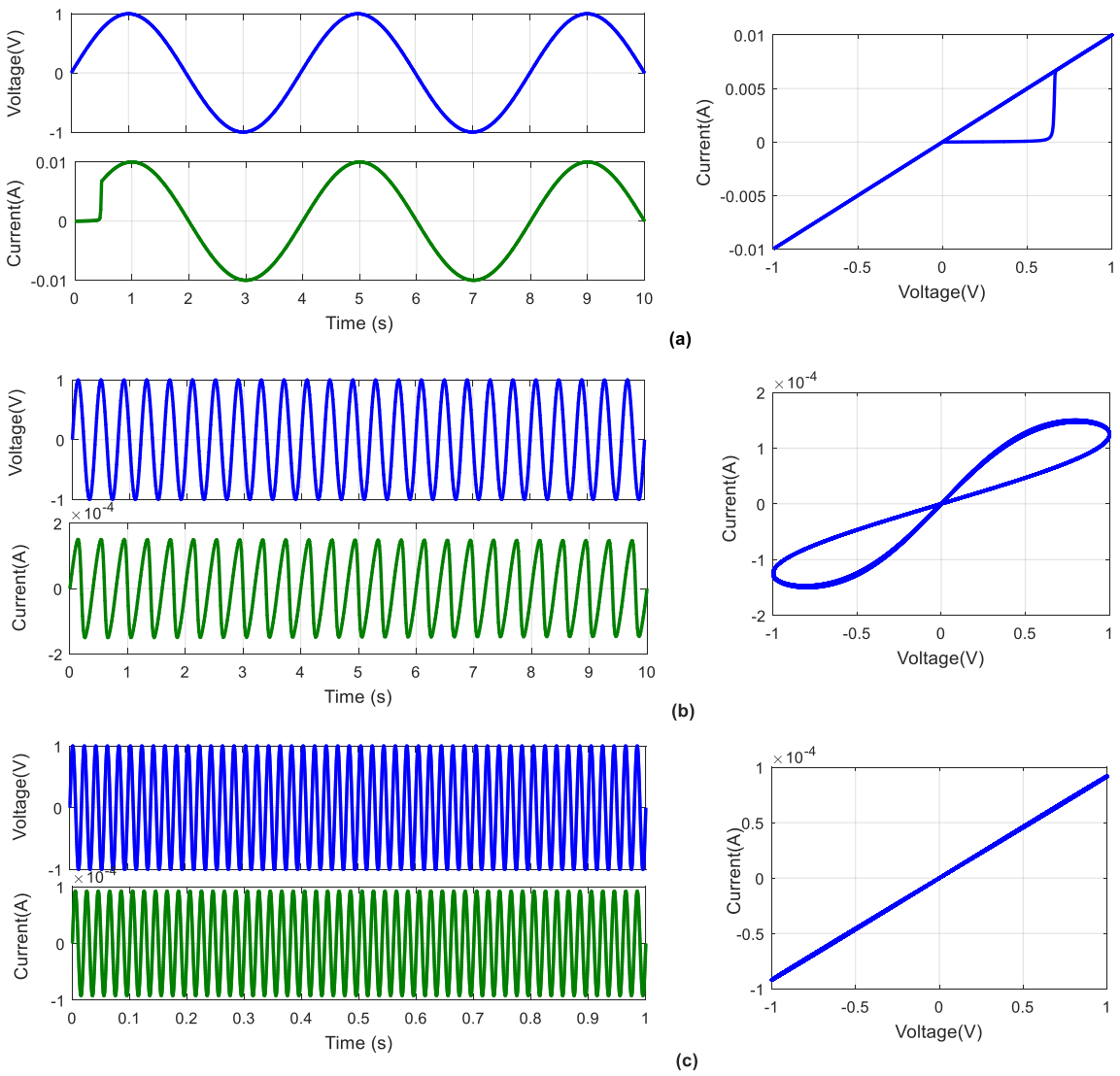


Figure 4. The input voltage /output current waveforms of the memristor element and its *v-i* characteristics for a) ω =0.25 rad/sec, b) 2.5rad/sec, c) ω =50 rad/sec.

As seen in Figure 4, almost no change has been observed at the output of the memristor element at $\omega_1=0.25$ *rad/s* value. A symmetrical hysteresis curve is observed at $\omega_2=2.5$ *rad/s*. Finally, when the sinusoidal input signal is $\omega_3=50$ *rad/s*, the memristor element behaves like a resistor and the phase portrait representation, which is drawn to observe the input/output relationship of the memristor, becomes a linear output like a resistor. Accordingly, it has been determined that it can be used a sinusoidal input signal at $\omega_2=2.5$ *rad/s* frequency to observe the characteristic

hysteresis curve of the memristor structure, that is designed by using the Joglekar window function for its hardware implementations on FPAA and FPGA platforms.

3. FPAA-based implementation of a Joglekar window function basedmemristor element

FPAA platforms are integrated circuits that offer stability, accuracy and rapid prototyping techniques in the design of analog/hybrid circuits. This platform contains basic analog operations and can be electrically reprogrammed to perform different analog functions. The FPAA platform consists of input/output ports, a logic control unit, and several configurable analog blocks called as CAB (Configurable Analog Block) that determine the memory of the element. In the designs where the memory of one FPAA board is not sufficient, these FPAA boards can be combined with each other [42]. Many of the analog operations take place in these CAB blocks and the switched capacitor technique is used for these operations. The system implemented on FPAA platform firstly is tested with a numerical analysis. This is because the FPAA device has a saturation level of ±2V. A rescaling procedure is applied to the parameters that exceed this saturation level. After rescaling, the predefined Configurable Analog Modules (CAM) blocks corresponding to the functions in the model are determined by utilizing the CAM block definition sheets. The interconnections between these CAM blocks are created on the interface program. The designed system is sent to the FPAA platform via serial port. The required measurements are recorded with an oscilloscope by using the input and output units on the board. AN231E04 platform produced by Anadigm Company has been used in this study. Anadigm Designer2 program is used to program this board. In this program, there are several predefined configurable analog blocks in order to perform various analog functions. The CAM blocks, which are used for the FPAA-based implementation of the Joglekar window function based memristor element, and the interconnections between these blocks are shown in Figure5. In this design, the following CAM blocks are used: SUMFILTER, TRANSFER FUNCTION, VOLTAGE, MULTIPLIER, DIVIDER, INTEGRATOR, HOLD, and OSCILLATOR.

$$\begin{aligned} v(t) &= \left[R_{on}x + R_{off}(1-x) \right] i(t) \\ M(x) &= R_{on}x + R_{off}(1-x) \end{aligned} \tag{9}$$

$$\frac{dx(t)}{dt} = ki(t)f(x)$$

$$f(x) = 1-(2x-1)^{2p}$$

In the numerical simulation where a sinusoidal input signal with $\omega=2.5$ *rad/s* and *1V* amplitude is applied to the input of this model. It is seen that the memristor value exceeds the saturation level. After the rescaling stage, the parameters in Eq.9 has been rewritten as $R_{on}=0.00625$, $R_{off}=1$, $k=2.47$ and the control parameter is set to onein the FPAA based implementation of this memristor element modeled with the Joglekar window function.

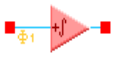
According to these calculations, the function $f(x)=1-(2x-1)^{2p}$ has been obtained by using the TRANSFER FUNCTION block. The memristance function, namely $M(x)=0.00625x+(1-x)$, has been constructed by using the SUMFILTER block. The velocity of the boundary between the doped region and the undoped region, which is given by the $dx(t)/dt=2.47i(t)f(x)$function, has been built by the MULTIPLIER block. A DIVIDER block has been used to obtain the current, namely $i(t)=v(t)/M(x)$. And finally, the $v(t)$ sinusoidal input signal has been implemented by using a OSCILLATOR block. The integration process has realized by the INTEGRATOR block. The HOLD block is used to regulate the phase state between the MULTIPLIER and DIVIDER blocks. The constant parameters in Eq.9 have been implemented by the VOLTAGE block that is a DC voltage source.



Figure 5. FPAA implementation diagram of the Joglekar window function based memristor element.

The CAM blocks used in the FPAA-based implementation of the Joglekar window function based memristor element are presented in Figure 5 and the parameter settings of these blocks are summarized in Table 1[42].

Table 1: A summary for the CAM blocks used in the FPAA-based implementation of the Joglekar window function based memristor element.

Block name	Options	Parameters	Description
SumFilter 	Output Changes On: *Phase 1* Input 1: *Non-inverting* Input 2: *Inverting* Input 3 : *Off*	Corner Frequency:*0.35* kHz Gain 1: *1.07* Gain 2: *1*	This CAM creates a summing stage with upto three inputs that includes a single pole low pass filter.
Integrator 	Polarity: *Non-inverting* Input Sampling Phase: *Phase 1* Compare Control To: *No Reset*	Integration Const. [1/us]:*0.05*	This CAM creates an integrator with a programmable integration constant.
Divider 	Sample and Hold: *Off*	Divider Factor : *0.34*	This CAM creates a divider.
Multiplier 	Sample and Hold: *Off*	Multiplication Factor : *2.5*	This CAM creates a multiplier.
Hold 	Input Sampling Phase : *Phase 1*		This CAM creates a sample and hold.
Transfer Function 	Output Hold : *Off*		This CAM implements a user specified voltage transfer function with 256 quantization steps.
OscillatorSine 		Osc. Frequency [kHz]: *0.85* Peak Amplitude [V]: *1.5*	This CAM creates a sinusoidal output, centered on signal ground. It has a programmable amplitude and frequency
Voltage 	Polarity : *+2V*		This CAM creates a connection to the on-chip voltage references.

The Joglekar window function based memristor element has been built with this interface program, easily. Then, it has been directly embedded in the AN231E04 board with a serial port and there is no need for any extra conversion. Finally, the experimental measurements have been recorded by digital oscilloscope for this analog memristive system. Figure 6.a shows the time domain representations: The signal in the top side is the sinusoidal signal *v(t)* that is applied to the input of the Joglekar window function based memristor element and the current signal measured through the memristor element is given in the bottom side in Figure 6.a. In Figure 6.b, the characteristic hysteresis curve of this memristor elementhas been obtained experimentally by the phase portrait representation and this representation has been formed by measuring the input sinusoidal signal *v(t)* against to the output current *i(t)*. Thus, a Joglekar window function based memristor element has been implemented with the FPAA platform, successfully. The FPAA-based realization results and the numerical simulation results are compatible with each other.

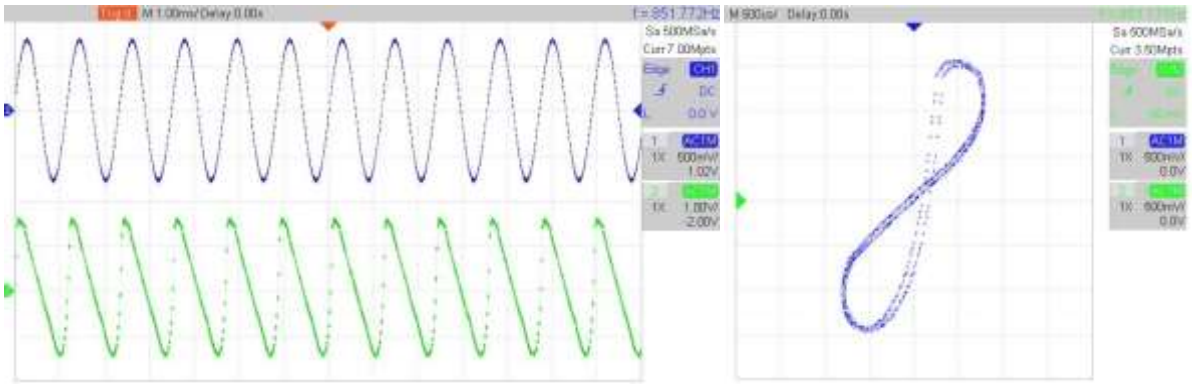


Figure 6. FPAA-based experimental realization results of a Joglekar window function based memristor element a) *v(t)* (top) and *i(t)* (bottom) input - output signals, b) *v(t)-i(t)* phase portrait representation.

4. FPGA-based implementation of a Joglekar window function basedmemristor element

The important studies on the memristor element in digital systems are focused on two basic categories: utilizing for building of the digital memories and designing the memristor emulators with the digital logic circuits. In the digital memory applications, the memristor acts as a switch thanks to its two-level resistor characteristic. If logic '0' and logic '1' values are assigned to two-level resistor, the memristor becomes a memory cell that can store 1-bit and represents

one of two possible outcomes of the Boolean function [43]. The studies, which are handled the usage effectiveness of the memristor element in different digital systems, are another application field. Generally, the programmable and reconfigurable digital devices are chosen in these studies to prove the effectiveness of this element and the Field Programmable Gate Array (FPGA) is one of the frequently used platforms in these applications.

FPGA device is a programmable and reconfigurable digital electronic platform consisting of the small digital blocks and interconnections between these blocks. FPGAs are digital ICs that operate in parallel and instantaneous ways contrary to systems with the standard processors. The FPGA device includes components such as the programmable input/output units, the programmable interconnections, the clock channels and the phase locked loops (PLLs), the memory units, the multipliers and the programmable logic blocks. The FPGAs use a programming language to implement the functions that perform certain operations similar to FPAAs, a software development program is recommended by the manufacturer in order to organize the interconnections between these created units. Discrete-time definitions are used in the designs on FPGAs. If a system has a continuous time definition, this system is redefined as a discrete time system by utilizing from the various discretization methods and the accuracy of this transformation is tested with the numerical simulations. The discretized system is modeled with a suitable interface program by using a hardware definition languages and it is embedded to the FPGA platform. The outputs of the FPGA are also digital, so its outputs are converted to the analog signals by using a Digital Analog Converter (DAC). The obtained experimental results can be measured from the output of a DAC via an oscilloscope.

In this study, Spartan-3AN platform produced by XILINX company was used. The programming of this FPGA platform is executed by the System Generator for DSP (SG_{DSP}) tool [44]. This tool is developed by XILINX Company and allows direct conversion from MATLAB to IP Core codes. The fixed-point definition, *Q(32,18)*, has been used in this design and a Joglekar window function based memristor element, which has a continuous time definition, has been converted to a discrete time definition by using the Euler discretization method as in the following equation:

$$
\begin{aligned}
&v(t) = M(x)i(t) \\
&M(x) = R_{on}x + R_{off}(1-x) \\
&x(t+1) = (\frac{\mu_v R_{on}}{D^2} i(t) f(x))\Delta h + x(t) \\
&f(x) = 1-(2x-1)^{2p}
\end{aligned}
\tag{10}
$$

The values of the parameters in Eq.10 have been chosen the same as the numerical simulations in the previous sections

In order to realize the *i(t)=v(t)/M(x)*expression, the dividing operation is not performed in the FPGA platform that is used in this study. To overcome this shortcoming, a current resource has been designed for applying to the input of the Joglekar window function based memristor element and the *v(t)=i(t)M(x)* expression has been able to be realized. Thus, the basic hysteresis characteristic can be observed successfully. This current source *i(t)* has been gotten as follows: Firstly, a Van Der Pol oscillator with oscillation frequency $\omega=1.25$ *rad/s* has been designed and the output voltage of this oscillator has been converted to a current signal by passing it through a resistor. The obtained current source has been defined by the $i(t)=v_{source}(t)/R_{source}$ relation. Here, the value of the R_{source} resistor is $20k\Omega$. Then, the voltage measurement has been recorded at the output of the memristor element by applying this current source to the memristor input. In fact that, $v_{source}(t)$-$v(t)$ measurement has been usedin order to observe the characteristic memristor hysteresis curve. After applying the Euler discretization method and the values of the parameters have been substituted in Eq.10, the final definition has been obtained as in Eq.11.

$$
\begin{aligned}
&v(t) = M(x)\frac{v_{source}(t)}{R_{source}} \\
&M(x) = 100x + 16000(1-x) \\
&x(t+1) = (\frac{30\times10^{-15}100}{(9\times10^{-9})^2}\frac{v_{source}(t)}{R_{source}} f(x))0.001 + x(t) \\
&f(x) = 1-(2x-1)^{2p}
\end{aligned}
\tag{11}
$$

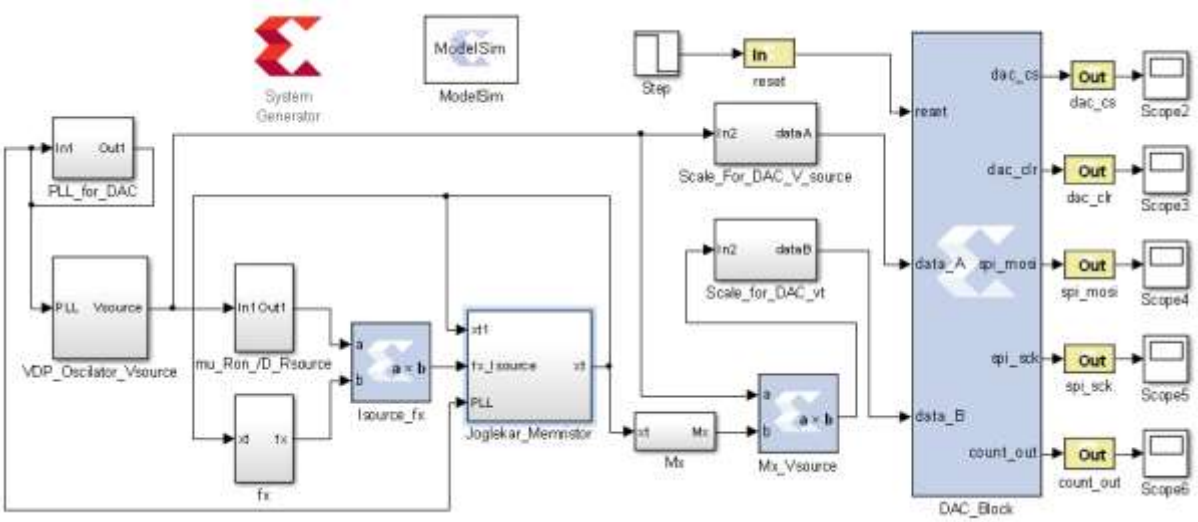


Figure 7. SG_{DSP}-based design diagram of the Joglekar window function based memristor element.

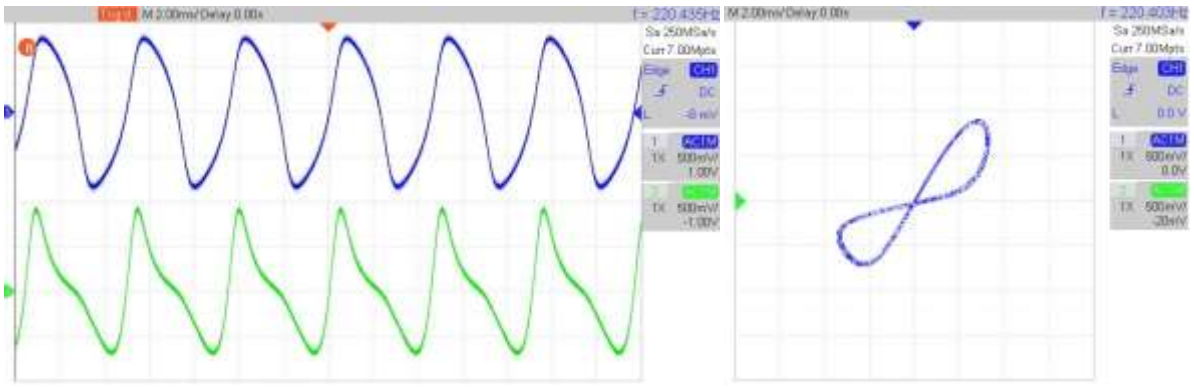


Figure 8. FPGA-based experimental realization results of the Joglekar window function based memristor model: a) $v_{source}(t)$ (top) and $v(t)$ (bottom) input-output signals, b) $v_{source}(t)$-$v(t)$a phase portraitillustration.

The designed schema in SG_{DSP} tool for the FPGA-based realization of the Joglekar window function based memristor element in Eq.11 is shown in Figure 7. This design has been converted to VHDL via the SG_{DSP} tool and the final IP cores have been embedded to the Spartan-3AN FPGA platform. The real-time experimental results have been measured through a DAC via a digital oscilloscope. These results are given in Figure 8. Figure 8.a shows the time domain representations of the $v_{source}(t)$ sinusoidal signal (top side) and the $v(t)$ voltage (bottom side) that is measured at the memristor output. In here, the $v_{source}(t)$ voltage is obtained by the

FPGA-based implementation of the VDP oscillator. This signal has been applied to the input of theJoglekar window function based memristor element and the measured $v(t)$ voltage has been recorded from the output of the memristor element. In Figure 8.b, the characteristic hysteresis curve has been observed with the phase portrait representation and this representation has been formed by plotting the $v_{source}(t)$ versus $v(t)$. Thus, the Joglekar window function based memristor element has been implemented with theFPGA platform, successfully.

5. Discussions

In the previous sections, the followed procedures in the FPAA and the FPGA based implementations of the Joglekar window function based memristor element have been detailed. The obtained results from these implementations are quite similar to the numerical simulations. However, these programmable and reconfigurable analog/digital devices have their intrinsic properties. For example, while the memristor element, which has a continuous time model definition, can be implemented with the analog FPAA element without any pre-conversion. This model has been discretized for its FPGA based implementation and this discretization process causes a low amount of errors in the model. The design procedure of a continuous system on the FPGA platform is more complex than on the FPAA platform. Additionally, DAC or ADC must be used in order to measure the results of the designed system in the FPGA based implementation process. On the other hand, the hardware capacities of each platform have been limited in the electronic designs. In order to compensate for limited memory problem, while FPAA platforms are able to combined each others, several different options of the FPGA platform are manufactured for various application fields. As mentioned in the introduction part, even though a direct comparison is impossible between these platforms, it is clear that the FPGA platforms have large memory capacity in the current technology. The hardware usage value of the FPAA and FPGA based implementations of the Joglekar window function based memristor element are summarized in Table 2 and 3, respectively.

Table 1. The synthesis results of the FPAA based implementation of the Joglekar window function based memristor element.

CAB1 (used/total capacity)	CAB2 (used/total capacity)	CAB3 (used/total capacity)	CAB4 (used/total capacity)	Power consumption
8/8	6/8	8/8	7/8	164±49mW

Table 2. The synthesis results of the FPGA based implementation of the Joglekar window function based memristor element.

Used/ Total Slice Registers	Used/ Total 4 input LUTs	Used/ Total Slices	Used/ Total BUFGMUXs	Used/ Total MULT18X18SIOs	Max Delay (ns)
137/11777 (1%)	1564/11776 (13%)	960/5888 (16%)	2/24 (8%)	16/20 (80%)	1.093

The analog FPAA and the digital FPGA platforms have their intrinsic software tools and these tools offer the opportunities for developing different projects. Thanks to these tools, the circuit edition process is maintained properly and robustly. The power consumptions of the FPAA and the FPGA based implementations of the Joglekar window function based memristor element have been elicited by using the development tools, namely, AnadigmDesigner2 and ISE Design Suite for FPAA and FPGA, respectively. While the power consumption is recorded as in Table 3 for the FPGA based design, the power consumption is 164±49mW for the FPAA based design. If the maximum operating frequency of these two platforms is considered, the FPAA has a limited performance. While the signal processing operation can be implemented up to 2MHz in FPAA platform, the FPGA platform is able to operate at higher frequencies depending on the used board.

Table 3. The power analyzer results of the FPGA based implementation of the Joglekar window function based memristor element.

	Clocks	Logic	Signals	MULTs	I/Os	Leakage	Total
Power Analyzer Results (W)	0.006	0	0.004	0.004	0	0.036	0.051

6. Conclusions

Programmable and reconfigurable analog/digital platforms have been offered an alternative perspective for realizing the nonlinear dynamical systems. In this study, the FPAA and FPGA based memristor emulator designs have been realized together in order to contribute the memristor-based analog and digital applications that is required real-time signals. In the initial stage of these realizations, while the Joglekar window function based memristor model has been rescaled because of the saturation level of the FPAA platform, this model has been discretized

because of the digital nature of the FPGA platform. In fact, this model has been subjected to a preliminary preparation process in both realizations. After the confirmation stage with numerical analysis results, the Joglekar window function based memristor model has been constructed on the software development tools of these programmable analog/digital platforms, separately and the constructed structures have been embedded to these platforms. While FPAA-based analog realization results can be measured directly without requiring additional equipment, FPGA-based realization results were obtained through a DAC. Therefore, the analog and the digital memristor emulators have been accomplished successfully with two programmable platforms and just one experimental setup as seen in Figure 9.

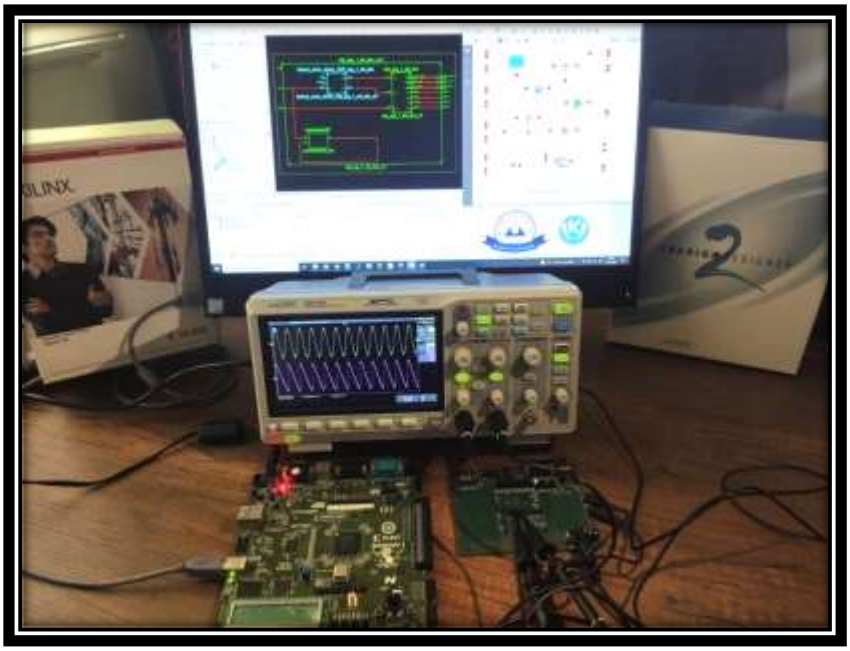


Figure 9. Experimental setup of the FPAA and the FPGA based realizations of the Joglekar window function based memristor model.

COMPLIANCE WITH ETHICAL STANDARDS

The authors declare that they have no conflict of interest.

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