Advanced Control of Positive Output Self-Lift Luo Converter Using Type-2 Fuzzy Neural Network via Elliptic Membership Function

2023 Innovations in Intelligent Systems and Applications Conference (ASYU) | 979-8-3503-0659-0/23/$31.00 ©2023 IEEE | DOI: 10.1109/ASYU58738.2023.10296827

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***Abstract*— In this paper, it is aimed to obtain an effective output voltage regulation performance from a positive output self-lift luo converter. For this purpose, firstly, a positive output self-lift luo converter was designed and an advanced control-based type-2 fuzzy neural network structure with elliptic type-2 fuzzy membership function was proposed to obtain an efficient output voltage regulation from the converter. The voltage regulation performance of the proposed voltage regulator was tested via comparative simulation studies using type-1 fuzzy neural network in MATLAB/Simulink environment in terms of voltage regulation response time such as settling and recovery times under three different operational conditions. The results of the comparative simulation studies demonstrated that the proposed voltage regulator displayed a faster voltage regulation response than type-1 fuzzy neural network voltage regulator.**

Keywords—Positive Output Self-Lift Luo Converter, Type-2 Fuzzy Neural Network, Elliptic Membership Function

I. INTRODUCTION

Positive output self-lift luo converters (POSLLCs) provide a positive low-ripple direct current (DC) output voltage, which overcomes parasitic effects that limit voltage transfer gain [1]. These converters have a non-linear circuit topology due to their switched nature. Since conventional proportional-integral (PI), proportional-derivative (PD) and proportional-integral-derivative (PID) controllers require a mathematical model of the system in the voltage regulation of these non-linear converter structures and are successful at certain operating points, they are still insufficient [2]. Therefore, in order to increase voltage regulation performance of these converters at different operating points, there is a need for intelligent controller structures such as fuzzy logic and artificial neural networks that do not require a mathematical model of the system to be controlled [3]. Fuzzy logic control systems are examined as two separate control structures: type-1 and type-2 [4]. The absence of certain rules in determining the exact values of membership functions and linguistic variables, which is one of the most important design features of type-1 fuzzy control systems, leads to complexity [5-6]. This complexity in modeling type-1 fuzzy control systems leads to uncertain situations. A more stable system response is obtained through an effective modeling of the uncertainties with type-2 fuzzy control. An adaptive control structure based on system predictions is provided by combining type-2 fuzzy control and artificial neural networks to create a single type-2 fuzzy neural controller structure [7]. In the existing literature, there are different sustainable energy applications and voltage regulation methods with POSLLCs [8-15], while the use of intelligent controllers is quite limited in applications with POSLLCs. In this paper, unlike the previous studies, the focus is on the type-2 fuzzy-neural control structure with elliptic type-2 fuzzy membership function (ET2FMF) for the voltage regulation of the POSLLC. Other parts of the paper can be summarized as follows: The circuit model of POSLLC is given in Section 2. T2FNN designed for voltage regulation of POSLLC is described in Section 3. Simulation studies and results of the the proposed voltage regulator are given in Section 4. Finally, the obtained results are concluded in Section 5.

II. CIRCUIT MODEL OF POSLLC

The POSLLC consists of a controlled semiconductor switching element, diode, inductor, capacitor and resistive load. The circuit model is given in Fig.1 [16].

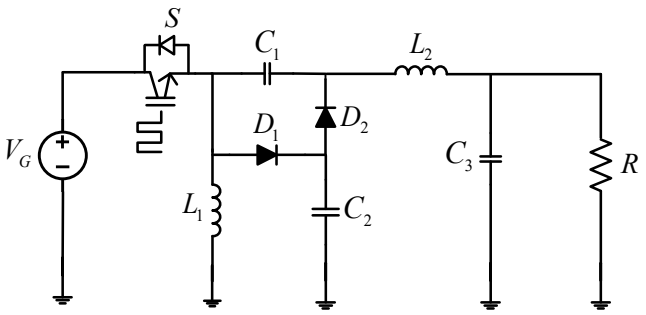


Fig.1. POSLLC circuit model

POSLLC operates in continuous conduction mode (CCM), the switching element (*S*) operates in ON or OFF modes and all circuit elements are ideal. When the switching element (*S*) is ON mode operation, the voltage of C_1 capacitor is equal to input voltage. Here, i_L inductor current increases until the operation of switch off mode. The equivalent circuit during switch on mode operation is shown in Fig. 2.

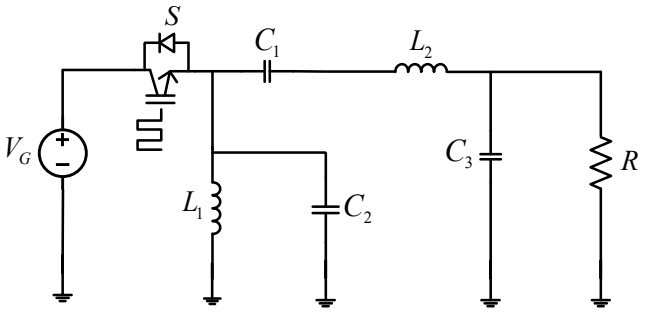


Fig.2. POSLLC equivalent circuit during switch on mode operation

Equation 1 can be written as follows for the equivalent circuit during switch on mode operation.

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$$V_0 = \frac{V_G}{1-D} \tag{1}$$

When the switching element (*S*) is OFF mode, the equivalent circuit during switch off mode is shown in Fig. 3.

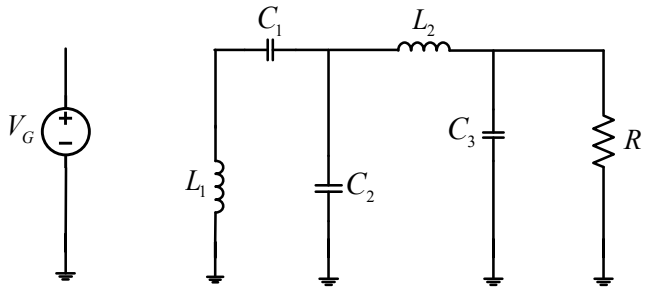


Fig.3. POSLLC equivalent circuit during switch off mode

During switch off mode, C_1 capacitor is charged with input voltage. The limit values of the POSLLC circuit element are calculated based on the change rates of the inductor currents and the capacitor voltages in equation 2-6. The variation ratio of current through the L_1 inductor can be calculated as:

$$\zeta_1 = \frac{\Delta I_{L_1}/2}{I_{L_1}} = \frac{R}{2M^2 f L_1} \tag{2}$$

Similarly, the variation ratio of current through L_2 inductor is given as:

$$\zeta_2 = \frac{\Delta I_{L_2}/2}{I_{L_2}} = \frac{DR}{2MfL_2} \tag{3}$$

The variation ratio of voltage across C_1 capacitor is expressed as:

$$\rho = \frac{\Delta V_{C_1}/2}{V_{C_1}} = \frac{D}{2fC_1R} \tag{4}$$

Similarly, the variation ratio of voltage across C_2 capacitor is calculated as:

$$\sigma_1 = \frac{\Delta V_{C_2}/2}{V_{C_2}} = \frac{M}{2fC_2R} \tag{5}$$

The variation ratio of voltage across C_3 capacitor can be given as:

$$\varepsilon = \frac{\Delta V_{C_3}/2}{V_{C_3}} = \frac{D}{8Mf^2L_2C_3} \tag{6}$$

Afterwards, the voltage transfer gain for a POSLLC in CCM is given in equation 7 [17].

$$M = \frac{V_0}{V_G} = \frac{1}{1-D} \tag{7}$$

The variation ratios of the current through L_1 and L_2 inductors are selected 10%, while the variation ratios of voltage across C_1, C_2 and C_3 capacitors are selected 0.625%, 2.5% and 0.0625% in this paper, respectively. Real converter element values should be selected higher than the calculated limited element values for CCM operation. The selected POSLLC element values for simulation studies are given in Table 1.

TABLE 1**.** The selected elementary POSLLC element values

Parameter	Symbol	Value
Inductor	L_1	10mH
Inductor	L_2	10mH
Capacitor	C_1	100µF
Capacitor	C_2	100µF
Capacitor	C_3	100µF
Resistive Load	R	100Ω
Input Voltage	V_G	20V
Output Power	P_0	64W
Output Voltage	V_0	80V
Switching Frequency	f	50kHz

III. VOLTAGE REGULATOR DESIGN BASED ON TYPE-2 FUZZY NEURAL NETWORK

As can be seen in Fig. 4, T2FNN based on first-order interval type-2 takagi-sugeno-kang (IT2TSK) fuzzy logic structure is preferred for this paper. In this structure, each rule can be expressed as follows:

$$\begin{aligned} &R_i : IF\ x_1\ is\ \tilde{B}_1^i \text{ and} \ldots \text{and}\ x_n\ is\ \tilde{B}_n^i \\ &\text{then } y_i = \tilde{b}_0^i + \sum_{j=1}^{n} \tilde{b}_j^i x_j, i = 1 \ldots M, j = 1 \ldots n \end{aligned} \tag{8}$$

Here, n is the number of the antecedents, $x_1, \ldots, x_n$ are input variables, M is the number of the rule, $\tilde{B}_1^i$`s represents interval fuzzy sets, and $\tilde{b}_j^i$`s indicates interval sets that symbolize the consequent parameters. Besides,

$$b_j^i = [c_j^i - s_j^i; c_j^i + s_j^i] \tag{9}$$

The description of c_j^i and s_j^i are given in the following section [18]. The internal structure of the T2FNN is shown in Fig.2. It can be divided into six layers with respect to the function of each layer.

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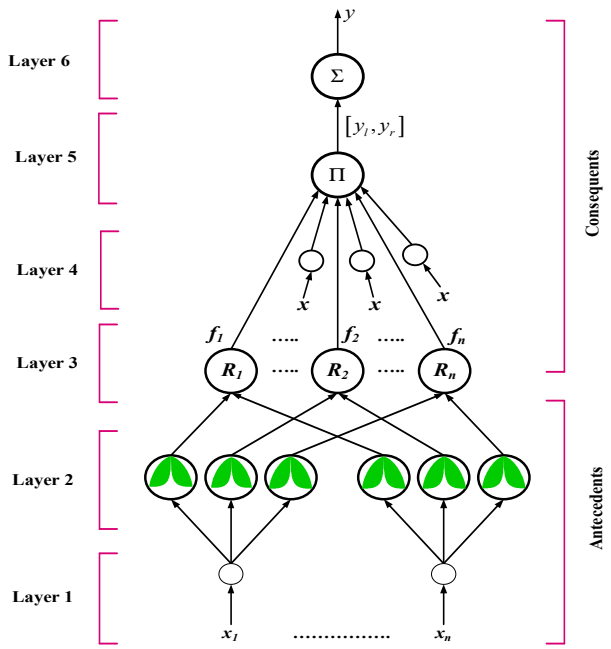


Fig. 4. Internal structure of T2FNN

The properties of each layer can be summarized as follows:

Layer 1: The input values are defined in this layer. These are also directly transferred to layer 2 and layer 4.

Layer 2: In this layer, the fuzzification process is carried out via elliptic type-2 fuzzy membership functions (ET2FMFs). Three ET2FMFs are used for each actual input, and ET2FMF can be formulated as follows:

$$\mu(x)=\left(1-\left|\frac{x-c}{z}\right|^{a}\right)^{1/a} \quad E(x,c,z) \quad a_2<a<a_1 \tag{10}$$

where c and z are the center and the width of the ET2FMF, and x is the input vector. The parameters a_1 and a_2 define the width of the uncertainty of the proposed ET2FMF, as follows:

$$\begin{aligned} &a_1=1.6\\ &0<a_2<1 \end{aligned} \tag{11}$$

a_1=1.6 and a_2=0.4 are selected in the present paper, and Fig.5 shows the shapes of the proposed ET2FMF [19].

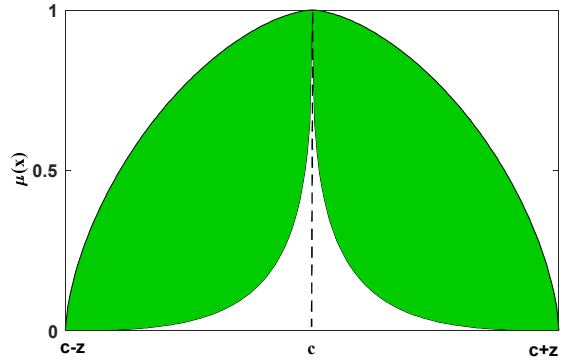


Fig.5. The shapes of the proposed ET2FMF

Layer 3: The firing strength of each fuzzy rule is computed in this layer. The computed firing strength can be expressed as follows:

$$F^i=\left[\underline{f}^i,\overline{f}^i\right] \tag{12}$$

$$\begin{aligned} \underline{f}^i&=\prod_{j=1}^{n}\underline{\mu}_j^i\\ \overline{f}^i&=\prod_{j=1}^{n}\overline{\mu}_j^i \end{aligned} \tag{13}$$

Layer 4: This layer is called TSK-type node. The output of each node is a type-1 fuzzy set, denoted by $[w_l^i, w_r^i]$, which can be computed as follows:

$$\begin{aligned} &\left[w_l^i,w_r^i\right]=\left[c_0^i-s_0^i,c_0^i+s_0^i\right]+\\ &\sum_{j=1}^{n}\left[c_j^i-s_j^i,c_j^i+s_j^i\right]x_j \end{aligned} \tag{14}$$

Layer 5: The output of this layer are combined with layer 3 and 4. The output of this layer can be calculated as follows:

$$\begin{aligned} y_l&=\frac{(1-q_l)\sum_{i=1}^{M}\underline{f}^i w_l^i+q_l\sum_{i=1}^{M}\overline{f}^i w_l^i}{\sum_{i=1}^{M}\underline{f}^i+\overline{f}^i}\\ y_r&=\frac{(1-q_r)\sum_{i=1}^{M}\overline{f}^i w_r^i+q_r\sum_{i=1}^{M}\underline{f}^i w_r^i}{\sum_{i=1}^{M}\underline{f}^i+\overline{f}^i} \end{aligned} \tag{15}$$

Here, q_l and q_r are called left and right design factor.

Layer 6: Finally, defuzzification is performed in this layer after calculating the value of $[y_l, y_r]$.

$$y=y_l+y_r \tag{16}$$

The gradient descent algorithm is used to update the antecedent and consequent parameters of T2FNN. The error of the output is first defined by the following equation:

$$E=\frac{1}{2}\sum_{i=1}^{O}(y_i^d-y_i)^2 \tag{17}$$

Here; the intended and actual output values of the T2FNN are symbolized using y_i^d , and y_i . c_j^i , z_j^i , w_j^i can be obtained via the equations given below:

$$c_j^i(k+1)=c_j^i(k)-\varphi\frac{\partial E}{\partial c_j^i(k)} \tag{18}$$

$$z_j^i(k+1)=z_j^i(k)-\varphi\frac{\partial E}{\partial z_j^i(k)} \tag{19}$$

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$$w_j^i(k+1) = w_j^i(k) - \varphi \frac{\partial E}{\partial w_j^i(k)} \quad (20)$$

Here, φ is the learning rate [20].

IV. SIMULATION STUDIES

The main objective of this section is to develop a T2FNN which can regulate in coordination with the changes in operational point of POSLLC. The overall control structure with POSLLC is shown in Fig. 6.

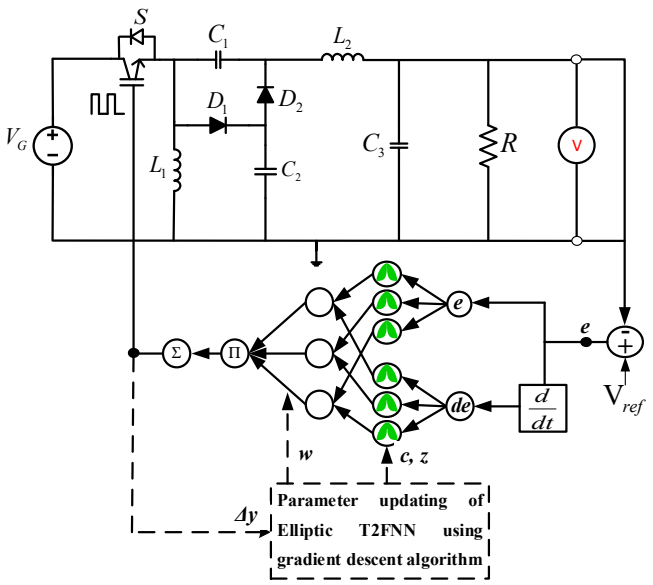


Fig.6.The overall control structure with POSLLC

According to Fig. 6, the control structure consists of two main blocks. The first block is T2FNN with two inputs (error signal (*e*) and change of error signal (*de*) and an output, i.e. the switching duty cycle (PWM). In our proposed control structure, the T2FNN uses the two inputs (*e* and *de*) to regulate the converter output voltage by adjusting the PWM. The second block is a parameter updating block where a gradient descent algorithm is used for updating the parameters of T2FNN through the output error (*E*). The input signal of updating block is the values of error (*E*), and its output signals are antecedent (*c,z*) and consequent (*w*) parameters of the T2FNN. The detailed simulation studies were performed in Matlab/Simulink environment to test the overall proposed control structure. Three different operating conditions are also included to regulate the output voltage of POSLLC for voltage regulators. These are summarized as follows:

Operational Condition 1:

In this operational condition, the dynamic performance of voltage regulators are examined with step set-point DC output reference (V_0) change. To this end, the reference DC output voltage is increased from 80V to 120V at 4s. Total simulation time lasted 8s, and sampling time was taken as 10µs. Comparative simulation results for step set-point reference voltage changes obtained from voltage regulators are given in Fig.7.

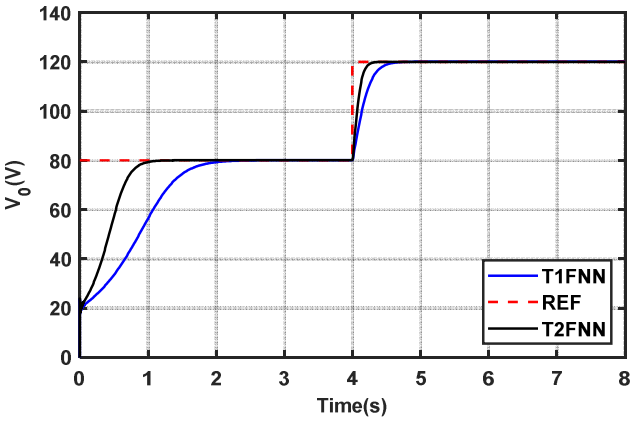


Fig.7. Comparative simulation results for step set-point reference voltage changes obtained from voltage regulators

As clearly shown in Fig. 7, step set-point reference output voltage change of POSLLC is nearly close to the set-point reference output voltages (80V and 125V) with all voltage regulators. In addition, the settling time performances of the proposed and T1FNN voltage regulator are 1.2s and 2.3s at set-point reference output voltage which is settled at 80V, respectively. Similarly, the settling time performances of the proposed and T1FNN voltage regulator are 0.33s and 0.72s at set-point reference output voltage which changed from 80V to 120V. When compared to T1FNN voltage regulator, the proposed voltage regulator improved settling time performance of the POSLL converter by 47.82% and 54.16% for all changes in set-point reference output voltage, respectively.

Operational Condition 2:

In this condition, the dynamic performance of voltage regulators are tested against different step set-point input (V_G) voltage values. In this respect, input voltage (V_G) value is increased from 20V to 25V at 4s. Total simulation time was 8s, and sampling time was taken as 10µs. Comparative simulation results for different input (V_G) voltage values obtained from voltage regulators are given in Fig.8.

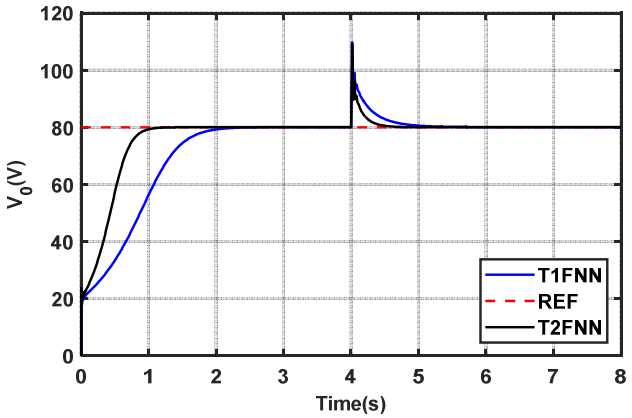


Fig.8. Comparative simulation results for different input (V_G) voltage values obtained from voltage regulators

It can be observed in Fig. 8 that after the input voltage (V_G) of POSLLC is increased from 20V to 25V at 4s, the recovery times of the proposed and T1FNN voltage regulators are calculated as 0.5s and 1s, respectively. Additionally, when

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compared to T1FNN voltage regulator, the proposed voltage regulator improved recovery time performance of POSLLC by 50% for changes in set-point input voltage.

Operational Condition 3:

In this condition, the dynamic performance of voltage regulators is measured to analyze different load resistance (R) values. Therefore, the load resistance of POSLLC is reduced from 100Ω to 50Ω at 4s. Total simulation time was 8s, and sampling time was taken as 10µs. Comparative simulation results for different load resistance (R) values obtained from voltage regulators are given in Fig.9.

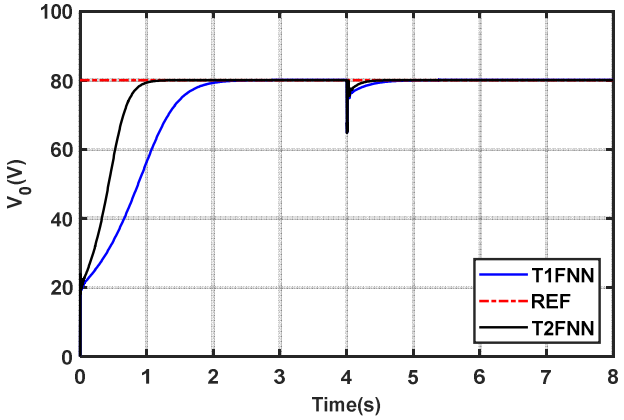


Fig.9. Comparative simulation results for different load resistance (R) values obtained from voltage regulators

According to Fig. 9, after the load resistance (R) of POSLLC is decreased from 100Ω to 50Ω, the recovery times of voltage regulators are calculated as 0.41s and 0.72s, respectively. As a result, compared to T1FNN voltage regulator, the proposed voltage regulator improved recovery time performance of POSLLC by 40.2% for different load (R) resistance values.

V. CONCLUSION

This paper proposed a new voltage regulator based on T2FNN to improve the dynamic performance of a POSLLC under different operating conditions. An ET2FMF was used to enhance voltage regulation performance of T2FNN. The obtained simulation results indicated that the proposed voltage regulator improved its durability for all different operational conditions and accelerated the voltage regulation response of the POSLLC. In future studies, it is aimed to tune the width of the ET2FMF in an adaptive manner to obtain a better voltage regulation performance of T2FNN.

ACKNOWLEDGEMENT

This paper was financially supported by the Kayseri University, Scientific Research Projects Unit, the project entitled “Development of Advanced Fuzzy Logic Based Control Methods for High Gain DC/DC Converter” under Project No: FKB-2022-1087.

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